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Advanced Through Silicon Via Technology for 3 Dimensional System-in-Package Fabrication

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論文内容要旨

Electronics industry is the most important industry that has led the development of modern civilization. As seen through the alteration of mobile phones, high density, small size, high speed and multifunctional electronic devices are required in electronics industry. Such a technical trend is the core factor that is leading a transition from 2D interconnection to 3D stacking technology. Until today, wire bonding technology is universally used for 3D stack packaging; this is due to its high yield rate and stabilized processes. However, wire bonding technology also contains problems such as performance drop due to electric interference between wires, constraints in high integration, and signal delays due to long wire paths. Therefore, the technology called through silicon via(TSV) recently standing out as a new solution. TSV is a technology that creates a hole within silicon, fills in conducting materials within the hole, and thereby making a direct vertical chip-to-chip connection. Compared with the widely used wire-bonding method, TSV has numerous advantages, including high density, electrical performance, signal speed, and low power consumption. It satisfies all the needs of electrical industries. Therefore, TSV is the most promising technology to satisfy the demands of the next generation. However, in spite of the advantages of TSV technology, TSV technology has not yet been applied to various fields. This is because of various obstacles including technical issues in manufacturing, reliability and expensive costs. Especially, the high costs factor is the greatest factor that is hampering commercialization of TSV technology, and the main reason for the high cost is the long filling time of the conventional via filling process. Furthermore, the conventional via filling process is complicated and also contains defects such as void. Thus, there is a considerable need for a low cost, defect-free via filling method.

Additionally, for implementation of TSV stack module, the joining of micro-bumps are highly essential processes in addition to TSV. As paradigm of electronic package technology shifts from 2D interconnection to 3D stack, wafer

thickness and joint size scale should be smaller. Therefore, in order to cope with the technological change, joining process using Cu pillar and solder cap bump is preferred to that of previous solder ball. However, as bump size and pitch size are getting smaller, the problem of solder bridging and bump misalignment occurred by using conventional flip-chip bonding technology. Also, as wafer thickness goes under 100um, problems such as handling and misalignment occurred due to slipping. Therefore, it became evident that bonding technology was required to solve these problems.

And the manufactured Sn-TSV and bump joint require a reliability assessment for checking applicability in 3D packaging. This is because reliability may decline after being exposed to heat during manufacturing process or usage. Conventional studies on Sn-TSV have mainly produced the result by using FEM simulation without support of experimental analyses. And also, as bump size becomes smaller by find-pitch trend of 3D stacking, IMC ratio increases dramatically due to relatively small amount of solder compared to solder bump and this can cause mechanical reliability issue by formation of kirkendall void. Therefore, the experimental evaluation of reliability on Sn-TSV and bump joint with Cu/Thin solder/Cu structure are required. Moreover, there is a clear need for a method for reliability improvements in order to resolve such reliability issues.

Therefore, in this study, new filling and bonding processes were studied to overcome the limitations of conventional technologies. This study further performed an evaluation on reliability and applicability of Sn-TSV for commercialization of TSV technology in 3D packaging. And finally, technologies for improving reliability of 3D stack module with Sn-TSV were proposed and studied.

In chapter 1 “Introduction”, the background and objectives of this study were described. Background, characteristic, fabrication process and technical/industrial trend and issue of TSV technology were mentioned. And the objective of this study was specified.

In chapter 2 “Advanced molten Sn filling process & evaluation”, the existing via filling processes was first reviewed and their issues were analyzed. And new molten solder filling technology with low-cost, high-speed and defect-free has been developed to overcome problems of conventional filling technology by achieving fast filling time, void-free and low pressure. Whereas existing filling technology used blind via for filling, through via used to fill molten solder in via by pressure difference of wafer both side in this research. Fig.1 shows the schematics of developed via filling technology in this research. Molten solder was spread on wafer with formed via. And then, molten solder was filled in via by using pressure difference caused by vacuum and solder pressurization. Via diameter were 10, 20 and 30um. Via depth was 110~210um. As a result, the new via filling technology was developed in a few seconds regardless of the via diameter with relatively low pressure and also minimized defects by using vacuum and solder pressurization, thereby ensuring high productivity and low cost in filling processes.

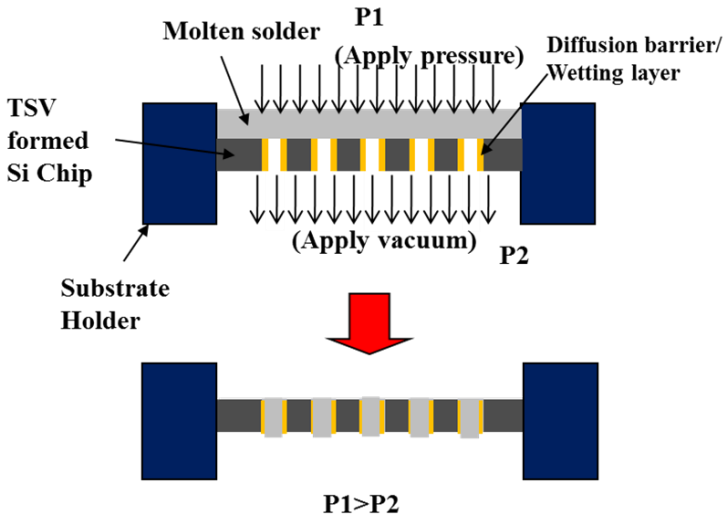

Fig. 1 Via filling of molten solder in through via by pressure difference

In chapter 3 "Micro-bump formation and joining process for 3D stacking", the existing bonding technology was reviewed and its problems were mentioned. And, a hybrid bonding technology was developed in order to improve the bonding accuracy with ultra-thin wafer (Thickness: <~100um) by self-alignment. And evaluation of factors that can affect self-alignment was performed. As a result, applied reflow process after flip-chip bonding completed high accuracy bonding of thin wafer with 50um thickness without solder bringing or bump misalignment due to self-alignment effect. And main factors of self-alignment were chip and solder bump volume. Therefore, based on research result, a bump design for 3D packaging is deemed possible. As another topic in this chapter, bonding characteristic of Sn-58Bi cap bump on Cu pillar was investigated for a low temperature stacking process. As a result, the bump joint by using Sn-Bi was formed in low temperature process but can cause reliability breakdown due to separated Bi and delamination at Cu/Solder/Cu's structure.

In chapter 4 "Evaluation of reliability and applicability of Sn-TSV on 3D stack process", the experimental evaluation on process applicability and thermal reliability of Sn-TSV and bump joint was performed for applicability verification in 3D stack technology. As a result of reflow test on Sn-TSV, around the temperature of 230℃, filled Sn began to melt but did not come out outside because it was locked by Cu pillar or pad. After three times of reflow, leaking problem did not appear and there was no change in microstructure. And thermal cycle test performed to observe Sn-TSV's thermal reliability. The Sn of via with 30um diameter came out gradually during thermal cycle; however, Sn extrusion of 20um diameter via was not observed after thermal cycle. Therefore, it is expected that proposed filling method can be applied to 3D TSV technology under 20um via without any reliability issue. And aging test was performed to bump joint reliability. At 150℃ and over 300h, entire solder turned into IMC and mechanical characteristic reduced by more than 90% by increase of kirkendall void ratio. Therefore, IMC

controlling technology at joint interface to improve reliability will be required.

In chapter 5 “Study on reliability improvement and applicability of Sn-TSV on 3D stack industry”, the research on improvement of reliability was performed. The variation and behavior of IMC growth by Ti interlayer were investigated for control of IMC growth in interface of Sn TSV-Cu pillar and bump joint. Ti interlayer was formed between Sn-TSV and Cu pillar bump. Ti thickness was 50, 100, 200 and 400nm respectively. Aging test was carried out at 150℃ for 500h. As the Ti layer thickness increased, the thickness of the IMC decreased. The IMC thickness affected shear strength of Cu pillar bump. Therefore, because IMC thickness affect mechanical properties of bump, adjusting of Ti layer thickness will improve TSV reliability. And also, for low CTE mismatch in TSV, fabrication of composite filling material was developed through mixing the ball-milled Sn-SiC clusters in molten solder. Sn powder and SiC nano particle were combined through the use of ball mill process to produce SiC-Sn cluster which resembles a ball shape and this was put in molten solder to develop SiC composite filling material. As a result, CTE of the composite solder was lowered as the amount of SiC increased up to 1wt%. Lowest CTE of SiC-Sn composite was 14.8um/m℃ which was lower than Cu. Therefore, it will be expected that it can be possible to improve TSV reliability.

Finally, in chapter 6 “Conclusion”, the researcher gave an overall summary and evaluation of the research. As mentioned above, the TSV technology is the best candidate for 3D stack packaging that exists today. However, in order for it to be applied to various fields, the cost must be lowered and numerous technical issues need to be resolved. Hence, in efforts to overcome such issues, this research has provided a total solution for future commercialization of TSV technology by proposing and developing some core TSV manufacturing process technologies, as well as conducting a comprehensive study on process applicability, reliability assessment and reliability improvement solutions. The low-cost, high-speed molten solder filling technology of this study will solve the current technical problem and lower the manufacturing cost of TSV, thereby greatly contributing to TSV chip productions. And the developed bump joining technology will increase the yield of 3D stack module. Consequently, such advanced technologies for 3D SiP manufacturing, along with reliability improvement technologies, will be utilized to apply and expand TSV technology to various fields in future.

論文審査結果の要旨

電子部品の大容量化・高速化には半導体の 3 次元化、すなわちシステムインパッケージの製造技術の確立が必須である。3 次元実装においては、シリコン貫通電極の利用が期待されているが、その製造効率や製品の信頼性に課題が残されている。本研究では、シリコン貫通電極を用いたシステムインパッケージ製造の実用化に不可欠となる高速精密溶融ろう充填技術、マイクロバンプ作製とその精密接合技術、熱疲労に強い長寿命で高信頼性ろう材などを開発することを目的としている。論文は全編 6 章で構成されている。

第 1 章は序論であり、本研究の背景および目的を述べている。

第 2 章では、シリコン貫通電極に高速で溶融 Sn ろうを充填する新しいプロセスを提案し、本プロセスの最適化ならびにろう材が充填されたシリコン貫通電極の評価等を行っている。その結果、シリコン貫通電極に高速で溶融ろうを充填するには、シリコン貫通電極の上に溶融ろうを配置し、上部からの加圧と下部からの真空引きにより圧力差を設けることが有効であることを示している。また、シリコン貫通電極中に充填された Sn ろう材には欠陥発生が少なく、高い信頼性を有することを示している。

第 3 章では、半導体の 3 次元積層に必要なマイクロバンプの精密接合において、表面エネルギーの最小化を利用した自己整列技術を提案し、本技術の最適化と支配因子について調べている。その結果、自己配列にはバンプとピラーの体積比が極めて重要であることを明らかにしている。

第 4 章では、Sn ろう材が充填されたシリコン貫通電極に対して熱サイクル試験を行い、ろう材の熱的安定性を実験的に調べている。その結果、微細なシリコン貫通電極が長時間の熱サイクルを付与しても高い信頼性を維持することを明らかにしている。

第 5 章では、半導体の 3 次元積層における更なる信頼性向上を目指して、バリア層による Sn ろう材/Cu ピラー間に生成する金属間化合物の抑制ならびにろう材の熱膨張率の最適化による熱応力の低減を試みている。その結果、Sn ろう/Cu ピラー間の反応を Ti バリア層により効果的に抑制し、Sn ろうへの炭化ケイ素の添加によりろう材の熱膨張係数をピラーに近づけることに成功している。

第 6 章は本研究の結果をまとめた総括である。

以上要するに本論文は、半導体実装における 3 次元システムインパッケージ製造のためのシリコン貫通電極において、実用的に有用な新技術を開発し、製造効率と製品の信頼性の向上に大きく貢献するものであり、材料システム工学の発展に寄与するところが少なくない。

よって、本論文を博士（工学）の学位論文として合格と認める。